REMARKS

Applicants have amended the claim set to further clarify points that Applicants assert were completely clear in the claim set prior to the present amendment. Thus, the present amendment is made merely to expedite allowance and move the case through to issuance and not due to any of the rejections set forth in the present Office Action.

That said, Applicants address the individual rejections made in the present Office Action.

Regarding the §112, second paragraph, rejection, Applicants assert that while the previous claims clearly addressed any vagueness or indefiniteness issues, the present claim set further defines the various PRBSs and from where they are generated, e.g., device under test, PRBS generator, etc.

Accordingly, withdrawal of the §112, second paragraph, rejection is respectfully requested.

Regarding the §103 rejection of claims 1, 6 and 11 based on the Lee reference alone, Applicants traverse same since the Lee reference fails to recite each and every limitation of independent claims 1, 6 and 11.

By way of example, assuming a first PRBS is generated at a PRBS generator, comprising a first shift register chain, and presented to a device under test, and the device under test generates a second PRBS in response to the first PRBS, Lee fails to delay the second PRBS in a second shift register chain that corresponds to the first shift register chain to generate a delayed second PRBS. This is because Lee is not a self-synchronizing PRBS checker.

Further, Lee does not detect the presence of an error bit in the second PRBS by comparing the delayed second PRBS at an intermediate point in the second shift register chain with the second PRBS.

The Examiner admits that Lee does not prohibit propagation of the detected error bit. The claim now further reads that prohibition is performed such that the detected error bit does not further propagate through the second shift register chain. This limitation is no where disclosed in Lee.

Regarding the §103 rejection of claim 12 based on the Ajima reference alone, Applicants traverse same since the Ajima reference fails to recite each and every limitation of independent claim 12.

By way of example, assuming an output pseudorandom bit sequence (PRBS) generated by a device under test in response to an input PRBS received by the device under test from a PRBS generator comprising a first shift register chain, Ajima fails to disclose a second shift register chain that corresponds to the first shift register chain. Again, Ajima is not a self-synchronizing PRBS checker.

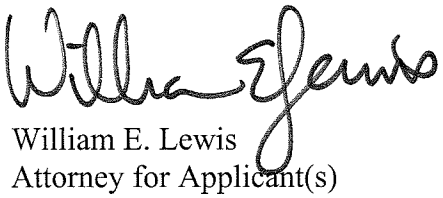
Thus, Ajima also fails to disclose a logic gate coupled to the second shift register chain and the device under test for detecting, for a given clock cycle, the presence of an error bit in the output PRBS generated by the device under test, the error bit representing a mismatch between the input PRBS generated by the PRBS generator and the output PRBS generated by the device under test.

Lastly, the Examiner admits that Ajima clearly does not disclose at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the second shift register chain.

No rejections other than the §112 rejection appear to have been made with respect to the dependent claims of the present application.

In view of the above, Applicants believe that claims 1-17 are in condition for allowance, and respectfully request withdrawal of the various §112 and §103(a) rejections.

Respectfully submitted,



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